

## CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
  - 2 a first device to transmit a plurality of data
  - 3 signals in parallel mode; and
  - 4 a second device coupled to receive the plurality of
  - 5 data signals from the transmitter circuit,
  - 6 wherein the second device detects phase information
  - 7 of each data signal against a corresponding clock signal
  - 8 and feed back the phase information to the first device,
  - 9 the first device adjusts an output delay of each data
  - 10 signal based on the phase information fed back from the
  - 11 second device.
- 1 2. The apparatus of claim 1 wherein the second device
  - 2 feeds back the phase information to the first device in
  - 3 serial mode.
- 1 3. The apparatus of claim 1 wherein the second device
  - 2 samples parallel data patterns transmitted from the first
  - 3 device and feeds back the sampled data to the first
  - 4 device.
- 1 4. The apparatus of claim 3 wherein the second device
  - 2 samples the parallel data patterns in response to a first
  - 3 command signal from the first device.

1 5. The apparatus of claim 3 wherein the second device  
2 feeds back the sampled data to the first device in serial  
3 mode.

1 6. The apparatus of claim 1 wherein the first device  
2 detects phase variations that are in excess of one bit of  
3 the sampled data fed back from the second device and  
4 shifts data bit positions between parallel data words to  
5 align phase variations that are in excess of one bit  
6 interval.

1 7. An apparatus comprising:

2 a first device to transmit a plurality of data  
3 signals in parallel format; and

4 a second device to receive the plurality of data  
5 signals from the first device,

6 wherein the second device detects phase information  
7 of each data signal with respect to a corresponding clock  
8 signal and adjusts a delay of the respective data signal  
9 based on the phase information detected prior to sampling  
10 of the data signals.

1 8. The apparatus of claim 7 wherein the second device  
2 transmits parallel data sample to the first device,  
3 subsequent to the sampling of the data signals.

1 9. The apparatus of claim 8 wherein the first device,  
2 upon receiving the parallel data sample from the second  
3 device, compares the parallel data sample to a programmed  
4 parallel data pattern.

1 10. The apparatus of claim 9 wherein the first device  
2 generates a signal to accompany data words being  
3 transmitted to the second device that match the programmed  
4 data pattern.

1 11. The apparatus of claim 10 wherein the second device,  
2 in response to the signal from the first device indicating  
3 a match to the programmed data pattern, recognizes phase  
4 variations that are in excess of one bit of the parallel  
5 data sample and shifts data bit positions between parallel  
6 data words to align phase variations that are in excess of  
7 one bit interval.

1 12. A method comprising:

2 transmitting a plurality of data signals in parallel  
3 mode from a first device to a second device over a first  
4 bus;

5 detecting phase information of each data signal  
6 received at the second device against a corresponding  
7 clock signal;

8 sending the phase information from the second device  
9 to the first device; and

10 adjusting an output delay of each data signal at the  
11 first device based on the phase information received from  
12 the second device.

1 13. The method of claim 12 wherein the phase information  
2 is sent from the second device to the first device in  
3 serial mode.

1 14. The method of claim 12 further including:  
2 sampling and holding, at the second device, parallel  
3 data pattern received from the first device;  
4 feeding back the sampled data from the second device  
5 to the first device;  
6 recognizing, at the first device, phase variations  
7 that are in excess of one bit of the sampled data fed back  
8 from the second device; and  
9 shifting data bit positions between parallel words to  
10 align phase variations that are in excess of one bit  
11 interval.

1 15. A method comprising:  
2 transmitting a plurality of data signals from a first  
3 device to a second device in parallel mode over a first  
4 bus;  
5 detecting, at the second device, phase information of  
6 each data signal with respect to a corresponding clock  
7 signal; and  
8 adjusting a delay of the respective data signal prior  
9 to sampling of the data signal at the second device.

1 16. The method of claim 15 further including:  
2 sending parallel data sample from the second device  
3 to the first device; and  
4 upon receiving the parallel data sample at the first  
5 device, comparing the parallel data sample with a  
6 programmed parallel data pattern.

1 17. The method of claim 16 further including:

2 generating, from the first device, a signal to  
3 accompany data words being transmitted to the second  
4 device that match the programmed data pattern.

1 18. The method of claim 17 further including:

2 in response to the signal from the first device that  
3 indicates a match to the programmed data pattern,  
4 recognizing phase variations that are in excess of one bit  
5 of the parallel data sample; and

6 adjusting data bit positions between parallel data  
7 words to align phase variations that are in excess of one  
8 bit interval.

1 19. A system comprising:

2 a processor;

3 a first component coupled to the processor; and

4 a second component coupled to the first component,

5 wherein the first component transmits data words to the

6 second component in parallel mode, each data word

7 including a plurality of data bits, wherein the second

8 component detects phase information of each data bit

9 relative to a corresponding clock signal and feeds back

10 the phase information of each data bit to the first

11 component, the first component adjusts an output delay of

12 each data bit based on the phase information fed back from

13 the second component.

1 20. The system of claim 19 wherein the second component  
2 samples parallel data patterns received from the first  
3 component and feeds back the sampled data patterns to the  
4 first component.

1 21. The system of claim 20 wherein the first component,  
2 based on the sampled data patterns fed back from the  
3 second component, recognizes phase variations that are in  
4 excess of one bit of the sampled data patterns fed back  
5 from the second component and adjust data bit positions  
6 between parallel data words to align phase variations that  
7 are in excess of one bit interval.

1 22. The system of claim 19 wherein the first component  
2 receives data words from the second component in parallel  
3 mode, each data words including a plurality of data bits,  
4 and wherein the first component detects phase information  
5 of each data bit relative to a corresponding clock signal  
6 and adjusts a delay of the respective data bit based on  
7 the phase information detected prior to sampling of the  
8 data bits.

1 23. The system of claim 22 wherein the first component  
2 transmits parallel data sample to the second component  
3 subsequent to the sampling of the data bits.

1 24. The system of claim 23 wherein, upon receiving the  
2 parallel data sample from the first component, the second  
3 component compares the parallel data sample to a  
4 programmed parallel data pattern and generates a signal to

5 accompany data words being transmitted to the first  
6 component that match the programmed data pattern.

1 25. A machine-readable medium comprising instructions  
2 which, when executed by a machine, cause the machine to  
3 perform operations including:

4 transmitting a plurality of data signals in parallel  
5 mode from a first device to a second device over a first  
6 bus;

7 detecting phase information of each data signal  
8 received at the second device against a corresponding  
9 clock signal;

10 sending the phase information from the second device  
11 to the first device; and

12 adjusting an output delay of each data signal at the  
13 first device based on the phase information received from  
14 the second device.

1 26. The machine-readable medium of claim 25 wherein the  
2 operations performed further including:

3 sampling and holding, at the second device, parallel  
4 data pattern received from the first device;

5 feeding back the sampled data from the second device  
6 to the first device;

7 recognizing, at the first device, phase variations  
8 that are in excess of one bit of the sampled data fed back  
9 from the second device; and

10       shifting data bit positions between parallel words to  
11 align phase variations that are in excess of one bit  
12 interval.

1   27. The machine-readable medium of claim 26 wherein the  
2 operations performed further including:

3       transmitting a plurality of data signals from the  
4 second device to the first device in parallel mode;

5       detecting, at the first device, phase information of  
6 each data signal with respect to a corresponding clock  
7 signal; and

8       adjusting a delay of the respective data signal prior  
9 to sampling of the data signal at the first device.

1   28. The machine-readable medium of claim 27 wherein the  
2 operations performed further including:

3       sending parallel data sample from the first device to  
4 the second device; and

5       upon receiving the parallel data sample at the second  
6 device, comparing the parallel data sample with a  
7 programmed parallel data pattern.

1   29. The machine-readable medium of claim 28 wherein the  
2 operations performed further including:

3       generating, from the second device, a signal to  
4 accompany data words being transmitted to the first device  
5 that match the programmed data pattern.

1   30. The machine-readable medium of claim 29 wherein the  
2 operations performed further including:



3           in response to the signal from the second device that  
4   indicates a match to the programmed data pattern,  
5   recognizing phase variations that are in excess of one bit  
6   of the parallel data sample; and  
7           adjusting, at the first device, data bit positions  
8   between parallel data words to align phase variations that  
9   are in excess of one bit interval.

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